AMENDMENT TO THE DRAWINGS

Please replace FIG. 3 of the Drawings with the attached, corrected FIG. 3. In the corrected FIG. 3, the device "Current Control 52" has been changed to "Current Selector 52" to coincide with the language of the Specification (see Present Application, page 8, ll. 3-31). It is respectfully submitted that no new matter is being introduced with the submission of corrected FIG. 3.

REMARKS

Claims 1-27 are currently pending in the subject application, and are presently under consideration. Claims 1-27 stand rejected. Claims 5-7, 9, 16, 17, 19, 20, 23, 24, 26, and 27 have been amended. New claims 28-31 have been added. Favorable reconsideration of the application is requested in view of the amendments and comments herein.

I. Rejection of Claims 1, 5-13, 16-20, 25, and 26 Under 35 U.S.C. §102(b)

Claims 1, 5-13, 16-20, 25, and 26 stand rejected under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 5, 017,919 to Hull, et al. ("Hull"). Claims 5-7, 9, 16, 17, 19, 20, and 26 have been amended. Withdrawal of this rejection is respectfully requested for at least the following reasons.

Claim 1 recites a first current source having a first configuration that is selectively adjusted to achieve a first current and a second current source having a second configuration that is selected to generate a second current that is a multiple of the first current in response to a selection of the first configuration. The Office Action dated December 15, 2005 ("Office Action"), asserts that Hull anticipates claim 1 on the basis of a low-order, current sourcing, interdigitated array 211 reading on the first current source; a high-order, current sourcing matrix 216 reading on the second current source; and an 8-bit digital signal presumably reading on the selective adjustment of the first and second current sources (Office Action, page 2). Representative for Applicant respectfully disagrees.

Hull teaches a digital-to-analog converter (DAC) that converts an 8-bit digital signal to an analog current signal (Hull, Abstract). The low-order, current sourcing, interdigitated array 211 generates fifteen separate unit currents that each mirror a reference current (Hull, col. 9, ll. 38-43). Of the fifteen unit currents, seven are input to a unit-current differential switch array 212 which selectively switches the unit currents to the DAC output (Hull, col. 9, ll. 44-49). The selective switching results from decoding three bits of the 8-bit digital signal (Hull, FIG. 1, col. 9, ll. 14-16, 21-23, and 44-49). Hull further teaches that the remaining eight of the unit currents are converted to biasing signals and input to the high-order, current sourcing matrix 216 (Hull,

col. 9, ll. 51-63). The high-order, current sourcing matrix 216 generates 31 multi-unit currents that are input to a multi-unit current differential switch matrix 218 which selectively switches the multi-unit currents to the DAC output (Hull, FIG. 1, col. 9, line 64 through col. 10, line 5).

It is respectfully submitted that neither the low-order, current sourcing, interdigitated array 211 nor the high-order, current sourcing matrix 216 are selectively adjusted to generate their respective currents, as asserted by the Office Action. Each of these current sources generate the respective fifteen and thirty-one current outputs based solely on the magnitude of the reference current, and are thus not selectively adjusted to achieve a first current and a second current, as recited in claim 1. In addition, as cited above, the 8-bit digital signal is used to switch these respective fifteen and thirty-one current outputs to the DAC output. Therefore, Hull teaches a system comprising a single current source, and not a first current source having a first configuration and a second current source having a second configuration, as recited in claim 1. Even assuming *arguendo* that the teachings of Hull indicate two separate, selectively adjusted current sources, the two portions of the 8-bit digital signal that switch the outputs are separate and distinct. In addition, at no point does Hull teach that the values of the 3-bit portion and 5 bit portion of the 8-bit digital signal change sequentially. Instead, the teachings of Hull indicate that the two portions of the 8-bit digital signal are simultaneously input to the DAC. Therefore, even if Hull is considered to teach two separate, selectively adjusted current sources, Hull still fails to teach a second current source having a second configuration that is selected to generate a second current in response to a selection of the first configuration, as recited in claim 1. Accordingly, for all of the above reasons, Hull does not anticipate claim 1 because it fails to teach each and every element of claim 1. Withdrawal of the rejection of claim 1, as well as claims 2-12 which depend therefrom, is respectfully requested.

Amended claim 5 depends from claim 1 and should be allowed for the reasons stated above. In addition, amended claim 5 recites that the first current source comprises a first set of binary weighted Field Effect Transistors (FETs) coupled to provide the first current and the second current source comprises a second set of binary weighted FETs coupled to provide the second current. Neither Hull nor any other cited art teaches a first current source comprising a

first set of binary weighted Field Effect Transistors (FETs) coupled to provide a first current and a second current source comprises a second set of binary weighted FETs coupled to provide a second current, as recited in amended claim 5. Accordingly, withdrawal of the rejection of claim 5, as well as claims 6-9 which depend therefrom, is respectfully requested.

Amended claim 7 depends from claim 5 and should be allowed for at least the reasons stated above regarding claims 1 and 5. In addition, claim 7 recites that the first set of binary weighted FETs and the second set of binary weighted FETs define a current station, and further comprising a plurality of additional first set of binary weighted FETs and additional second set of binary weighted FETs defining a plurality of current stations. It is respectfully submitted that the Office Action does not address the language of original claim 7 as filed in its rejection of claims 1, 5-13, 16-20, 25, and 26 under 35 U.S.C. §102(b). Representative for Applicant respectfully submits that Hull does not teach amended claim 7. Withdrawal of the rejection of claim 7 is respectfully requested.

Claim 8 depends from claim 7 and should be allowed for at least the reasons stated above regarding claims 1, 5, and 7. In addition, claim 8 recites that the plurality of current stations are distributed at different locations across an integrated circuit, such that the second current is drawn more uniformly across the integrated circuit. It is respectfully submitted that the Office Action is deficient because it does not address the language of claim 8 in any way in its rejection of claims 1, 5-13, 16-20, 25, and 26 under 35 U.S.C. §102(b). Representative for Applicant respectfully submits that Hull does not teach claim 8. Withdrawal of the rejection of claim 8 is respectfully requested.

Amended claim 9 depends from claim 5 and should be allowed for at least the reasons stated above regarding claims 1 and 5. In addition, amended claim 9 recites a drain voltage offset compensator that compensates for a difference in drain voltage between the first and second sets of FETs. It is respectfully submitted that the Office Action is deficient because it does not address the language of pre-amended claim 9 in any way in its rejection of claims 1, 5-13, 16-20, 25, and 26 under 35 U.S.C. §102(b). Representative for Applicant respectfully

submits that Hull does not teach amended claim 9. Withdrawal of the rejection of claim 9 is respectfully requested.

Claim 12 depends from claim 1 and should be allowed for at least the reasons stated above regarding claim 1. In addition, claim 12 recites a charge rationing system that employs the second current to calibrate the charge rationing system by measuring the difference with the second current source in an "OFF" state and the second current source in an "ON" state. It is respectfully submitted that the Office Action is deficient because it does not address the language of claim 12 in any way in its rejection of claims 1, 5-13, 16-20, 25, and 26 under 35 U.S.C. §102(b). Representative for Applicant respectfully submits that Hull does not teach claim 12. Withdrawal of the rejection of claim 12 is respectfully requested.

Claim 13 recites a first set of semiconductor devices configured to provide a variable current source that generates a first current based on a first binary selection signal, a second set of semiconductor devices configured to provide a variable current source that generates a second current based on a second binary selection signal, and a control device that determines the value of the first current and sets the second binary selection signal to provide the second current that is a multiple of the first current. For the reasons described above regarding claim 1, Hull does not anticipate claim 13. In addition, Hull further does not teach a control device that determines the value of the first current and sets the second binary selection signal to provide the second current that is a multiple of the first current. The Office Action asserts that Hull teaches a control device by the microprocessor that provides the 8-bit control signal (Office Action, page 2, citing Hull, col. 8, ll. 42-59). Representative for Applicant respectfully disagrees. The microprocessor taught by Hull merely provides the 8-bit control signal to the DAC to generate a corresponding analog signal (Hull, col. 8, ll. 48-50). Assuming *arguendo* that the teachings of Hull indicate two separate, selectively adjusted current sources (see comments above regarding claim 1), Hull further does not teach that the microprocessor determines the value of the first current and sets the second binary selection signal to provide the second current, as recited in claim 13. As described above, the separate portions of the 8-bit control signal are separate and distinct. Accordingly, Hull does not anticipate claim 13 because it does not teach each and every

element of claim 13. Withdrawal of the rejection of claim 13, as well as claims 14-19, is respectfully requested.

Amended claim 16 depends from claim 13 and should be allowed for at least the reasons described above regarding claim 13. In addition, amended claim 16 recites the first set of semiconductor devices comprising a first set of binary weighted FETs coupled to provide the first current and the second set of semiconductor devices comprising a second set of binary weighted FETs coupled to provide the second current. Neither Hull nor any other cited art teaches the first set of semiconductor devices comprising a first set of binary weighted FETs coupled to provide the first current and the second set of semiconductor devices comprising a second set of binary weighted FETs coupled to provide the second current, as recited in amended claim 16. Accordingly, withdrawal of the rejection of claim 16, as well as claims 17-19 which depend therefrom, is respectfully requested.

Amended claim 17 depends from amended claim 16 and should be allowed for at least the reasons described above regarding claims 13 and 16. In addition, amended claim 17 recites a drain voltage offset compensator having at least one current correction factor to compensate for different drain voltages associated with the first set of binary weighted FETs and the second set of binary weighted FETs, the controller employs the at least one current correction factor to determine an actual second current associated with the second variable current source. For the reasons described above regarding claim 9, Hull does not anticipate claim 17. Withdrawal of the rejection of claim 17, as well as claims 18 and 19 which depend therefrom, is respectfully requested.

Claim 18 depends from claim 17 and should be allowed for at least the reasons described above regarding claims 13, 16, and 17. In addition, claim 18 recites that the drain voltage offset compensator comprises a drain voltage compensation table. Hull does not teach a drain voltage compensation table, and thus does not anticipate claim 18. Withdrawal of the rejection of claim 18 is respectfully requested.

Amended claim 19 depends from claim 18 and should be allowed for at least the reasons described above regarding claims 13 and 16-18. In addition, amended claim 19 recites a

plurality of current stations, each of the current stations having a first set of FETs and a second set of FETs, the plurality of current stations being distributed at different locations across the integrated circuit. As described above regarding claims 7 and 8, Hull does not anticipate amended claim 19. Withdrawal of the rejection of claim 19 is respectfully requested.

Claim 20 recites means for generating a first current, means for selectively adjusting the first current to achieve a desired first current, and means for selecting a desired second current based on the achieved desired first current. Claim 20 further recites means for generating a second current that is a multiple of the first current, and means for compensating for differences in voltages associated with powering the means for generating a first current and the means for generating a second current. For at least the reasons described above regarding claims 1 and 9, Hull does not anticipate claim 20. In addition, Hull does not teach that the switching of the unit-current differential switch array 212 and the multi-unit-current differential switch matrix 218 are in response to one another, or that they are sequential in any way. Therefore, assuming *arguendo* that the teachings of Hull indicate two separate, selectively adjusted current sources (see comments above regarding claim 1), Hull further does not teach means for selecting a desired second current based on the achieved desired first current, as recited in claim 20. Furthermore, for the reasons described above regarding claim 9, Hull does not teach means for compensating for differences in voltages associated with powering the means for generating a first current and the means for generating a second current, as recited in claim 20. Accordingly, Hull does not anticipate claim 20. Withdrawal of the rejection of claim 20, as well as claim 21 which depends therefrom, is respectfully requested.

Claim 25 recites a plurality of current stations distributed over different locations on an integrated circuit, each of the plurality of current stations having a first set of semiconductor devices and a second set of semiconductor devices. Claim 25 also recites a first select signal associated with selecting a first current to be sourced by the first set of semiconductor devices and a second select signal associated with selecting a second current to be sourced by the second set of semiconductor devices. Claim 25 further recites a current selector that controls the state of the first select signal and the second select signal and selects the first current sourced by the first

set of semiconductor devices and the second current source by the second set of semiconductor devices. For the reasons described above regarding claims 1, 7, and 8, Hull does not anticipate claim 25. Withdrawal of the rejection of claim 25, as well as claims 26 and 27 which depend therefrom, is respectfully requested.

Amended claim 26 depends from claim 25 and should be allowed for the reasons stated above. In addition, amended claim 26 recites that the first set of semiconductor devices comprises a first set of binary weighted FETs coupled to provide the first current and the second set of semiconductor devices comprises a second set of binary weighted FETs coupled to provide the second current. Neither Hull nor any other cited art teaches a first set of semiconductor devices comprising a first set of binary weighted FETs coupled to provide a first current and a second set of semiconductor devices comprises a second set of binary weighted FETs coupled to provide a second current, as recited in amended claim 26. Accordingly, withdrawal of the rejection of claim 26, as well as claim 27 which depends therefrom, is respectfully requested.

For the reasons described above, claims 1, 5-13, 16-20, 25, and 26 should be patentable over the cited art. Accordingly, withdrawal of this rejection is respectfully requested.

II. Rejection of Claims 2-4, 14, 15, 21-24, and 27 Under 35 U.S.C. §103(a)

Claims 2-4, 14, 15, 21-24, and 27 stands rejected under 35 U.S.C. §103(a) as being unpatentable over Hull in view of U.S. Patent No. 4,231,020 to Azzis, et al. ("Azzis"). Claims 23, 24, and 27 have been amended. Withdrawal of this rejection is respectfully requested for at least the following reasons.

Claim 2 recites a precision resistor coupled between the first current source and a fixed reference voltage. Claim 2 depends from claim 1. As described above, Hull does not teach a first and a second current source that are selectively adjusted to achieve a first current and a second current, respectively, as recited in claim 1. Also as described above, Hull teaches a system comprising a single current source, and not a first current source having a first configuration and a second current source having a second configuration, as recited in claim 1. Hull further fails to teach a second current source having a second configuration that is selected

to generate a second current in response to a selection of the first configuration, as recited in claim 1. Azzis teaches a DAC with n binary current sources and n two-way switches, n being the number of input word bits (Azzis, Abstract). However, the addition of Azzis does not cure the deficiencies of Hull to teach or suggest claim 1, from which claim 2 depends. Accordingly, neither Hull nor Azzis, individually or in combination, teaches or suggests claim 2. Withdrawal of the rejection of claim 2, as well as claims 3 and 4 which depend therefrom, is respectfully requested.

Claim 3 depends from claim 2 and should be allowed for at least the reasons described above regarding claim 2. In addition, claim 3 recites a current selector that determines the first current based on the voltage drop across the precision resistor and selectively adjusts the first current selection signal to a desired first current. The Office Action asserts that Azzis teaches a method of determining the value of currents to be applied and current corrections by utilizing voltage and resistance across resistors (Office Action, page 3). Representative for Applicant respectfully disagrees.

Azzis teaches a scaling circuit that has four resistors, R1-R4 (Azzis, col. 4, ll. 43-44 and 54-55). Azzis further teaches a low-order scaling circuit that has two resistors, R5 and R6 (Azzis, col. 4, ll. 63-67). The magnitude of current for master/slave current sources, as taught by Azzis, is determined by ratios of given pairs of the resistors R1 and R2, and R5 and R6. For example, Azzis teaches that "the values of currents provided by auxiliary sources 5, 6, and 7...can be modified provided that the values of the resistors forming the R1/R2 ratio are modified accordingly," (Azzis, col. 6, ll. 4-9), and "the current carried by conductor 19 is equal to the current carried by conductor 18 and multiplied by the ratio R5/R6," (Azzis, col. 5, ll. 7-10). Thus, Azzis teaches a group of resistors having values of resistance that are application specific to determine currents based on resistor pair ratios. In addition, Azzis teaches the following:

> Resistance R3 is used for summing the currents since it is connected between a voltage $+V_{REF}$ and output 10. The maximum output voltage is equal to V_{REF} when there is no bit current in output line 14. The resistances forming the R1/R4

> ratio are chosen so that the dynamics of the output signal are equal to $2V_{REF}$. This gives a minimum output voltage $-V_{REF}$ when all the currents are summed in resistor R3. (Azzis, col. 6, ll. 10-18).

This passage indicates that the voltage at the output of the DAC is determined from the number of currents from digital bit designations that are being switched to the output, and not the other way around. In other words, Azzis teaches that, at the output of the DAC, a voltage across the resistor R3 is determined based on the current arriving at the output node, and thus does not teach that a current is based on the voltage drop across a precision resistor, as recited in claim 3.

In addition, Azzis further fails to teach selectively adjusting a current to a desired current based on a voltage drop across a resistor. Azzis teaches that each bit of the digital signal to be converted to analog has an associated switching circuit that is controlled by the respective bit, as well as a force signal and an inhibit signal (see, *e.g.*, Azzis, FIG. 1). It is the switching of currents through the switching circuits into the output node that determines the voltage drop across the output resistor, according to the teachings of Azzis (see, *e.g.*, Azzis, col. 6, ll. 10-18). Therefore, Azzis does not teach or suggest selectively adjusting a current to a desired current based on a voltage drop across a resistor, as recited in claim 3.

Representative for Applicant further respectfully submits that claim 3 is non-obvious for one of ordinary skill in view of the teachings of Hull and Azzis. As described above with reference to claim 1, Hull fails to teach selective adjustment of the current signal. Also, as described above with reference to claim 20, Hull further fails to teach selective adjustment to a desired current. In addition, as described above, Azzis fails to teach or suggest selectively adjusting a current to a desired current based on a voltage drop across a resistor. Therefore, it is respectfully submitted that it would not be obvious to achieve selectively adjusting a current to a desired current based on a voltage drop across a resistor, as recited in claim 3, by combining the teachings of Hull and Azzis. Therefore, the combination of Hull and Azzis fails to teach or suggest claim 3. Withdrawal of the rejection of claim 3, as well as claim 4 which depends therefrom, is respectfully requested.

Claim 14 depends from claim 13. As described above regarding claim 13, Hull fails to teach a first set of semiconductor devices configured to provide a variable current source that generates a first current based on a first binary selection signal, a second set of semiconductor devices configured to provide a variable current source that generates a second current based on a second binary selection signal, and a control device that determines the value of the first current and sets the second binary selection signal to provide the second current that is a multiple of the first current, as recited in claim 13, from which claim 14 depends. The addition of Azzis does not cure the deficiencies of Hull to teach or suggest claim 13, from which claim 14 depends. Accordingly, neither Hull nor Azzis, individually or in combination, teaches or suggests claim 14. Withdrawal of the rejection of claim 14 is respectfully requested.

Claim 15 also depends from claim 13 and should be allowable for at least the reasons described above regarding claim 14. In addition, claim 15 recites that the control device determines the value of the first current by measuring the voltage across the precision resistor and determines the current flowing through the precision resistor based on the measured voltage and resistance of the precision resistor. For the reasons described above regarding claim 3, claim 15 should also be allowed over the cited art. Withdrawal of the rejection of claim 15 is respectfully requested.

Claim 21 depends from claim 20. As described above, Hull fails to teach means for generating a first current, means for selectively adjusting the first current to achieve a desired first current, and means for selecting a desired second current based on the achieved desired first current, as recited in claim 20, from which claim 21 depends. Also as described above, Hull further fails to teach means for generating a second current that is a multiple of the first current, and means for compensating for differences in voltages associated with powering the means for generating a first current and the means for generating a second current, as also recited in claim 20, from which claim 21 depends. The addition of Azzis does not cure the deficiencies of Hull to teach or suggest claim 20, from which claim 21 depends. Accordingly, neither Hull nor Azzis, individually or in combination, teaches or suggests claim 21. In addition, claim 21 recites that the means for selectively adjusting the first current to achieve a desired first current comprising

means for measuring a voltage across a precision resistor coupled to a fixed reference voltage and the means for generating a first current, and means for evaluating the first current based on the measured voltage and resistance of the precision resistor. For the reasons stated above regarding claim 3, claim 21 should further be allowed over the cited art. Withdrawal of the rejection of claim 21 is respectfully requested.

Claim 22 recites generating a first current through a precision resistor, determining the value of the first current by measuring the voltage across the precision resistor and evaluating the value of the first current based on the measured voltage and resistance of the precision resistor. Claim 22 further recites selectively adjusting the first current and determining the value of the first current until a desired first current is achieved, and generating a second current that has a value that is a multiple of the achieved first current. For the reasons described above regarding claim 3, claim 22 should be allowed over the cited art. Withdrawal of the rejection of claim 22, as well as claims 23 and 24 which depend therefrom, is respectfully requested.

Amended claim 23 depends from claim 22 and should be allowed for at least the reasons stated above regarding claim 22. In addition, amended claim 22 recites that the generating a first current comprising selecting at least one FET of a first set of binary weighted FETs, and the generating a second current comprising selecting at least one matching FET from a second set of binary weighted FETs, the at least one FET of the first set of binary weighted FETs and the at least one matching FET from the second set of binary weighted FETs having a substantially similar binary weighting. As stated above regarding amended claim 5, neither Hull nor any other cited art teaches or that the generating a first current comprising selecting at least one FET of a first set of binary weighted FETs, and the generating a second current comprising selecting at least one matching FET from a second set of binary weighted FETs, the at least one FET of the first set of binary weighted FETs and the at least one matching FET from the second set of binary weighted FETs having a substantially similar binary weighting. The addition of Azzis does not cure the deficiencies of Hull to teach this element. Therefore, neither Hull nor Azzis, individually or in combination, teach or suggest amended claim 23. Withdrawal of the rejection of claim 23 is respectfully requested.

Claim 27 depends from claim 25. As described above regarding claim 25, Hull fails to teach a plurality of current stations distributed over different locations on an integrated circuit, each of the plurality of current stations having a first set of semiconductor devices and a second set of semiconductor devices, as recited in claim 25. Also as described above regarding claim 25, Hull also fails to teach a first select signal associated with selecting a first current to be sourced by the first set of semiconductor devices and a second select signal associated with selecting a second current to be sourced by the second set of semiconductor devices, as recited in claim 25. In addition, Hull further fails to teach a current selector that controls the state of the first select signal and the second select signal and selects the first current sourced by the first set of semiconductor devices and the second current source by the second set of semiconductor devices, as recited in claim 25. The addition of Azzis does not cure the deficiencies of Hull to teach or suggest claim 25, from which claim 27 depends. Accordingly, neither Hull nor Azzis, individually or in combination, teaches or suggests claim 27. Withdrawal of the rejection of claim 27 is respectfully requested.

For the reasons described above, claims 2-4, 14, 15, 21-24, and 27 should be patentable over the cited art. Accordingly, withdrawal of this rejection is respectfully requested.

III. New Claims 28-31

New claim 28 depends from claim 6 and should be allowed for at least the reasons described above regarding claims 1 and 5. In addition, new claim 28 recites that the first set of binary weighted FETs and the associated matching FETs from the second set of binary weighted FETs are respectively activated by a first binary selection signal and a second binary selection signal, the first binary selection signal and the second binary selection signal each being a substantially similar N-bit word upon selection of the first configuration. None of the cited art teaches or suggests new claim 28. Consideration and allowance of new claim 28 is respectfully requested.

New claim 29 depends from claim 13 and should be allowed for at least the reasons described above regarding claim 13. In addition, new claim 29 recites that the first binary

selection signal and the second binary selection signal are each binary N-bit words, and wherein the control device sets the value of each of the first binary selection signal and the second binary selection signal to be substantially similar upon determining the value of the first current. None of the cited art teaches or suggests new claim 29. Consideration and allowance of new claim 29 is respectfully requested.

New claim 30 depends from claim 23 and should be allowed for at least the reasons described above regarding claims 22 and 23. In addition, new claim 30 recites that the generating the first current comprises activating a first N-bit binary selection signal to select the at least one FET of the first set of binary weighted FETs and the generating the second current comprises activating a second N-bit binary selection signal to select the at least one matching FET of the second set of binary weighted FETs, the first N-bit binary selection signal and the second N-bit binary selection signal being substantially similar. None of the cited art teaches or suggests new claim 30. Consideration and allowance of new claim 30 is respectfully requested.

New claim 31 depends from claim 26 and should be allowed for at least the reasons described above regarding claims 25 and 26. In addition, new claim 31 recites that the first select signal is a first N-bit binary signal that activates at least one FET from the first set of binary weighted FETs, and the second select signal is a second N-bit binary signal that activates at least one associated matching FET from the second set of binary weighted FETs, the first N-bit binary signal and the second N-bit binary signal having substantially similar values. None of the cited art teaches or suggests new claim 31. Consideration and allowance of new claim 31 is respectfully requested.

CONCLUSION

In view of the foregoing remarks, Applicant respectfully submits that the present application is in condition for allowance. Applicant respectfully requests reconsideration of this application and that the application be passed to issue.

Should the Examiner have any questions concerning this paper, the Examiner is invited and encouraged to contact Applicant's undersigned attorney at (216) 621-2234, Ext. 104.

No additional fees should be due for this response. In the event any fees are due in connection with the filing of this document, the Commissioner is authorized to charge those fees to Deposit Account No. 08-2025.

Respectfully submitted,

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